A K BAND DRO IN COPLANAR LAYOUT WITH DRY AND WET ETCHED InP HEMTs

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ABSTRACT

A DRO operating in the frequency range of 23.2-24.8 GHz was designed using InGaAs/InAlAs/InP HEMTs with dry and wet etched gate recess. The oscillator consisted of an MMIC in coplanar waveguide technology and an externally coupled mechanically tunable DR mounted on a microstrip line. An output power of 12 dBm and a phase noise of -107 dBc/Hz at 100 kHz offset from the carrier were measured. The achieved power efficiency was 21%.

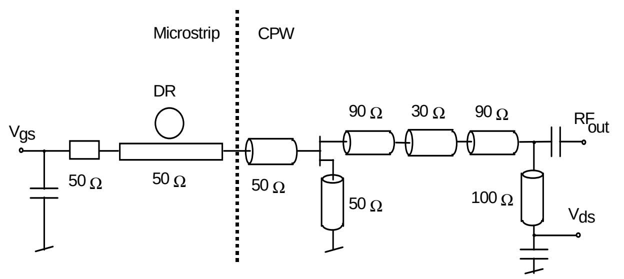

Figure 1: Topology of the negative impedance DRO

INTRODUCTION

With recent advances in transistor and microwave integrated circuit technology, it has become possible to realize fully integrated communication systems in the K band such as receiver front ends, Doppler modules and motion radars. These applications require highly stable RF sources with low phase noise and high output power. Dielectric resonator oscillators (DRO) are suitable candidates to meet these requirements [1],[2].

Most of the presented circuits are either hybrid mounted oscillators or monolithic microstrip DROs on GaAs substrate. In this work, we present a monolithic InP HEMT coplanar oscillator circuit connected to a duroid microstrip line which couples to the dielectric resonator (DR). This allows to reduce the area of InP substrate required to minimize substrate costs. The microstrip line ensures optimal coupling to the TE_{01} mode of the dielectric DR. The critical transition from microstrip to coplanar waveguide (CPW) has been investigated in order to achieve optimum resonator performance.

The active devices are lattice matched InGaAs/InAlAs/InP HEMTs with dry and wet etched gate recesses. Dry etched devices exhibit more reliable and uniform electrical parameters compared to wet etched devices. Both transistor types show comparable microwave noise characteristics [3]. The 1/f noise of the active devices mainly determines the phase noise of the oscillator [4],[5]. Our measurements showed lower 1/f noise for dry etched HEMTs compared to wet etched ones. Thus lower phase noise levels for oscillators using dry etched devices were observed.

The fabricated DRO circuits show state of the art performance. The output power at 24.1 GHz is 12 dBm and the phase noise is -107 dBc/Hz at

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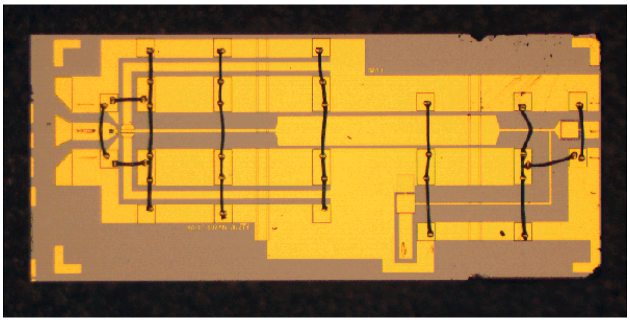


Figure 2: Photograph of the active MMIC oscillator chip (size 1.2x3 mm^2)

100 kHz offset from the carrier. These values are superior to those previously published [1],[6].

CIRCUIT DESIGN

The topology of the negative impedance resonator is shown in Figure 1. Linear circuit simulations were used for design. The active devices have a gate width of 2x75 µm and gate length of 0.2 µm. The maximum stable gain was 17 dB at the design frequency of 24 GHz. The CPW line models have been verified by measurements on

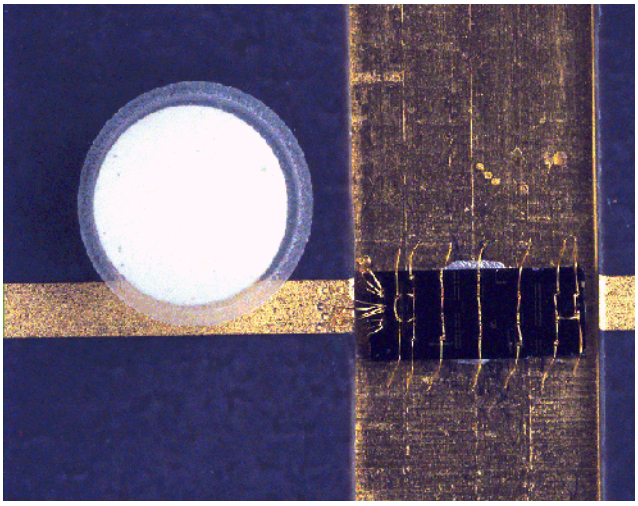


Figure 3: Photograph of the complete DRO

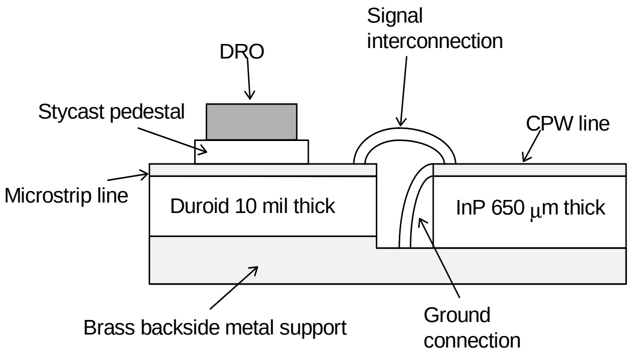


Figure 4: Schematic cross-section of the microstrip-CPW transition (not to scale)

passive test structures. The output matching has been achieved using stepped impedance lines of 30 Ω and 90 Ω. Figure 2 shows a photograph of the active MMIC oscillator chip in CPW technology on InP. The chip size is 1.2x3 mm^2. CPW technology is used since via holes and wafer thinning for microstrips are not required. On-wafer testing of subcircuits using ground-signal-ground probes is an additional advantage. The ground-ground spacing of the coplanar lines is 200 µm. The bias networks and coupling capacitances are integrated on the chip.

The DR was placed on a 50 Ω microstrip line fabricated on 10 mil thick Duroid substrate with a dielectric constant of 2.2. In order to minimize losses in the backside metallization, the DR was mounted on a 0.3 mm thick Stycast pedestal with a low loss tangent of 0.0005 and a dielectric constant of 2.54. The loaded Q_l of the mounted DR was measured to be 198. The unloaded Q_u factor of the DR was simulated to be around 4000. The DR was modeled by an RLC parallel resonant circuit. The complete DRO together with the interconnection between the microstrip line and the CPW of the active chip and the DR in place is shown in Figure 3. A cross-section of the transition from the microstrip to the CPW line can be seen in Figure 4. The transition was modeled

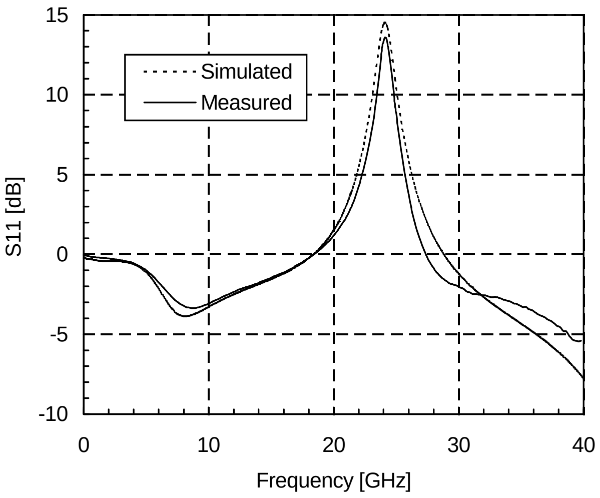
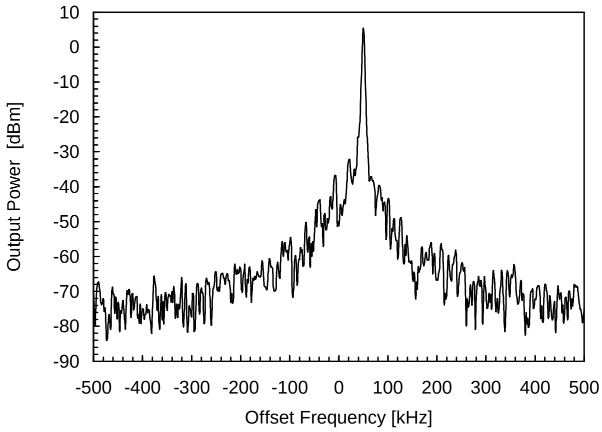


Figure 5: Simulated and measured input reflection of the active chip

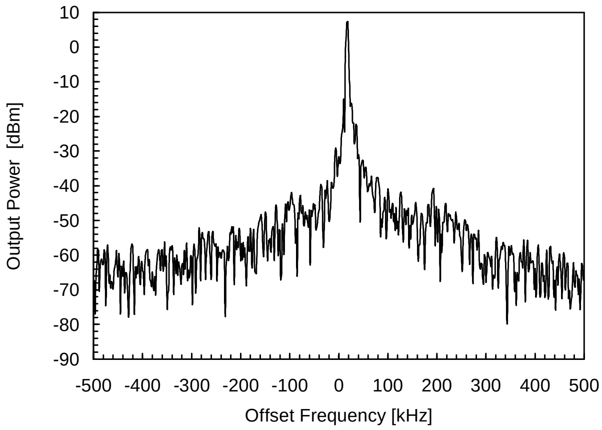
using an LC network. The complete DRO was simulated including the models for the DR and the microstrip-CPW transition.

MEASUREMENTS

The oscillator circuits were first measured without DR. Figure 5 shows the simulated and measured input reflection coefficient S_{11} of the active chip. The good agreement of the data indicates adequate modeling of the CPW lines. Measurements of the microstrip to CPW transition showed that the transition alone has 12 dB return loss, the 50 Ω load resistor has more than 20 dB return loss, and the return loss peak with the dielectric resonator in place is 5 dB.



a)



b)

Figure 6: Spectra of realized DROs, resolution bandwidth = 3 kHz. a): DRO with dry etched HEMT, center frequency = 24.16 GHz. b): DRO with wet etched HEMT, center frequency = 24.23 GHz.

Typical spectra of DROs with dry and wet etched HEMTs are shown in Figure 6 a) and b). No spurious oscillations could be detected in the frequency range from 0 to 50 GHz. The maximum output power was 12 dBm at a drain voltage of 4 V. The efficiency at this bias point was 21%. The phase noise showed no dependence on the drain bias and hence on the output power. The measured phase noise at 100 kHz offset from the carrier was -107 dBc/Hz for the dry etched DROs and -98 dBc/Hz for the wet etched ones. Three devices of each type have shown similar results. The difference is attributed to the lower 1/f noise level in dry etched HEMTs.

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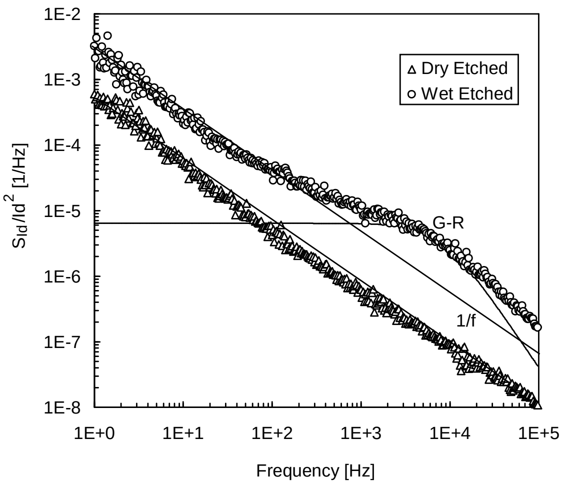

Figure 7: Normalized low frequency drain current noise spectra of dry and wet etched HEMTs (U_{ds} = 1 V, T = 300 K) [7]

Figure 7 shows the normalized low frequency noise spectra for dry and wet etched devices in the saturation region at a drain bias voltage of 1 V. The 1/f noise component with a slope of -1 and the Lorentzian-shaped noise component of a generation-recombination (G-R) center active at room temperature can be distinguished. The 1/f noise is considerably lower for the dry etched HEMT [7].

CONCLUSIONS

A monolithic DRO operating in the K band has been demonstrated. The active part in CPW technology and the DR coupling line in microstrip technology was accurately modeled. An output power of 12 dBm and a phase noise of -107 dBc/Hz at 100 kHz offset from the carrier could be achieved using dry etched HEMTs. The phase noise of the DROs using wet recessed devices was almost 10 dB higher at 100 kHz offset. Together with the higher controllability of plasma etching, this work shows the feasibility of dry etching techniques for phase noise sensitive applications.

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